A Stable, Low-Noise Crystal Oscillator for Microwave and Millimeter-Wave Transverters

Would you like to try narrow-band modes in the gigahertz bands? If so, you'll need a very stable and ultra-clean local oscillator. This project fills that need.

By John Stephensen, KD6OZH

Amateurs are using narrow-band modulation—including CW, SSB and NBFM—on ever-higher frequencies. In the US, SSB is commonplace on all microwave bands through 10 GHz and is spreading to the 24- and 47-GHz millimeter-wave bands. In Europe, narrow-band operation has taken place as high as 411 GHz.[1]

The local oscillator (LO) used at these higher, millimeter-wave frequencies must be much more stable than at lower microwave frequencies. On SSB, the indicated frequency should be within 500 Hz at both the transmitter and receiver, or you may not hear the station calling you. During a microwave contest, you don't want to adjust both the antenna *and* the frequency while trying to make a contact. I wasted many hours during the last 10-GHz-and-Up contest because the LO in my transverter was 85 kHz off frequency at 24.192 GHz.

A lesser-known problem is phase noise. When extended to millimeter-wave bands, most published LO designs for amateur microwave transverters have excessive phase noise that limits the dynamic range of the transverter. Many contesters on mountaintops have experienced this desensitization from commercial equipment on nearby frequencies or amateur beacons operating at the same site.

I decided to replace the LO in my 24-GHz transverter and solve both the phase-noise and stability problems. This article describes the crystal oscillator and multiplier designs that resulted. They work nicely with existing transverters using the KK7B LO design[2] with a few modifications and can be adapted to others. The KK7B LO was originally designed for a 2304-MHz transverter and was extended by N1BWT (now W1GHZ) with an additional ×5 multiplier for his 10-GHz transverter.[3] Replacing the original LO with the circuit described here and modifying the first multiplier board make this technology much

[1]Notes appear on page 17.

153 S Gretna Green Way
Los Angeles, CA 90049
kd6ozh@amsat.org

more usable on the millimeter-wave bands at 24 GHz and above.

The Phase Noise Problem Explained

The LO for a microwave or millimeter-wave transverter is usually a crystal oscillator operating around 100 MHz, which is then multiplied up to the amateur band in use. It is critical that this oscillator have a very low noise floor because each stage of multiplication adds noise to the signal at a rate of 6 dB each time the frequency doubles. In addition, the frequency multiplication process is lossy; signal levels can decrease rapidly with high-order multiplication, and the noise inherent in low-level amplifiers can degrade the noise floor even faster. Multiplying the crystal frequency by 100 to reach 10 GHz increases the noise floor by at least 40 dB. At 250 GHz, the added noise would be 68 dB, or more.

Many VHF crystal oscillator circuits have a noise floor no better than –155 dBc/Hz. This means that noise 155 decibels below the carrier power will appear in each hertz of bandwidth at the oscillator output. Multiplying to 245 GHz increases this to at least –87 dBc/Hz. This is the best case, and the degradation will always be several decibels worse due to the noise figure of components within the multiplier chain.

The problem with a high LO noise floor is that signals outside the receiver passband mix with this noise and appear as increased noise within the passband, reducing sensitivity. If NBFM is being used, the noise that appears in the 16-kHz bandwidth will be –87 + 42, only 45 dB below the level of the interfering signal: The receiver dynamic range is 45 dB. Therefore, any signal appearing within the passband of the RF circuitry (several gigahertz wide) that is 45 dB (about 7½ S-units) stronger than the desired signal will mask it completely. When transmitting, broadband noise will be radiated that is only 45 dB below your signal. The problem is smaller at lower frequencies but still results in a receiver that is easily overloaded. The same example at 10 GHz results in a 71-dB dynamic range, which is more acceptable, but still 15 dB worse than most VHF/UHF transceivers and more than 30 dB worse than many HF transceivers.

Improving Stability

The first issue is frequency stability. Quartz crystals have inherent temperature sensitivity that can vary the resonant frequency by ±10 ppm from 0 to +70°C, which amounts to ±100 kHz at 10 GHz. Temperature-compensated crystal oscillators and those in ovens do better at ±0.3 ppm or ±3kHz at 10 GHz. This is totally unacceptable at millimeter-wave frequencies, where the drift is multiplied to ±7 kHz at 24 GHz or ±75 kHz at 250 GHz.

To provide a rock-stable LO, the only solution is to phase lock the crystal oscillator to something more stable. Small rubidium frequency standards are now available at moderate cost on the surplus market. Typically, they are removed from obsolete radio-navigation equipment.[4] The long-term accuracy over temperature is 1 part in 10^9 or 0.001 ppm. This results in an accuracy of ±250 Hz after multiplication to the highest amateur band at 241-250 GHz.

Improving Phase Noise

The phase-noise problem is solved by building a crystal oscillator with a lower noise floor. The ratio of the noise at the input of the transistor to the signal arriving from the crystal ultimately determines this noise-floor level.

The traditional common-base Butler oscillator described in *The ARRL UHF/Microwave Experimenter's Manual* (see Fig 1) shows the problem. The input resistance of the 2N5179 emitter is very low ($26/I_e$ Ω). With the transistor biased for 5 mA emitter current, as shown, the input impedance is approximately 5 Ω. At resonance, the fifth-overtone crystals used in this circuit have a series resistance of about 60 Ω. In this type of oscillator, the peak current through the crystal is approximately equal to the standing current; the RMS current through the crystal is 3.5 mA, and the power dissipated in the crystal is I^2R or 0.735 mW.

The trouble is that the amount of power appearing at the 2N5179 emitter is only $(0.0035)^2(5)$ = 0.061 mW or –12 dBm, and the noise figure of the 2N5179 is probably about 10 dB in this configuration. The noise floor can be calculated by taking the noise power caused by circuit resistance, –177 dBm, adding the noise figure and subtracting input power level. This yields –177 + 10 – (–12) = –155 dBc. This is only a first-order estimate, and the actual oscillator could be several decibels worse.

The power level in the crystal cannot be raised, as it would cause excessive aging and instability. We must provide more input to the transistor by increasing its input impedance to provide a better match to the crystal. With a bipolar transistor amplifier, this means reducing the emitter current; but this would also reduce the power available, exacerbating the problem.

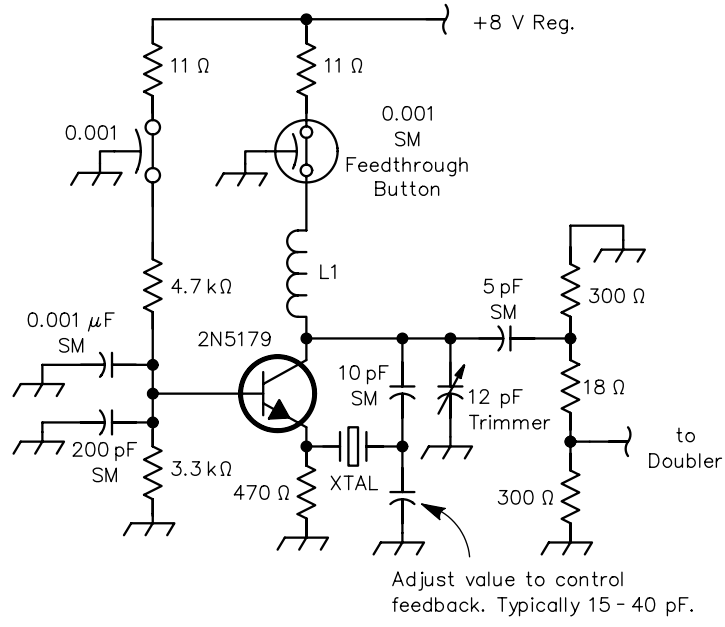

Fig 1—Conventional Butler Oscillator

The input impedance of a common-gate FET is the inverse of the transconductance and is independent of the standing current. The transconductance for a J310 FET is about 8,000-18,000 μS; its input impedance in a common-gate configuration is, therefore between 56 and 125 Ω. It also has a noise figure of less than 2 dB at 100 MHz. Replacing the 2N5179 with a J310 and keeping the same crystal dissipation results in an input power of $(0.0035)^2(56) = 0.686$ mW or –2 dBm in the worst case (lowest input impedance). We can also assume that the J310 noise figure may be degraded somewhat, to 3 dB, by noise in later stages. The noise floor is lowered to –177 + 3 – (–2) = –172 dBc—an improvement of 17 dB.

The increased input impedance does have one drawback: It is in series with the crystal, so the loaded Q of the crystal is lower than with a low-input-impedance circuit. In this application, it is not a problem. The motional capacitance of a 90 to 100-MHz crystal is about 2.4 fF (femtofarads), which results in a reactance of about 1.6 MΩ. The unloaded Q is about 27,000 (1,600,000/60) and the loaded Q is about 8700 in the worst case (1,600,000/(60+125)). This results in a bandwidth of about 11 kHz, which is fine for SSB and CW operation. To ensure that there is no additional degradation in Q, the crystal must be driven from a low-impedance source.

Once we have a low-phase-noise oscillator, we need to make sure that it is not degraded by succeeding stages in the LO chain. The amplifier(s) immediately following the VCXO must contribute very little noise, and the initial frequency multiplication must be done in small increments to minimize reduction of the LO level at any intermediate point. As the multiplication process proceeds, the LO noise floor rises. As it does, we can be less stringent in our requirements by using higher-order multipliers and having less constraint on noise figure.

The VCXO Circuit

The basis of the low-noise, phase-locked crystal oscillator (LNPLXO) is the voltage-controlled crystal oscillator (VCXO) circuit shown in Fig 2.

A J310 JFET (Q1) is a common-gate amplifier providing a high-impedance input for the signal from the crystal (Y1). A 2N5179 bipolar transistor (Q2) is an emitter follower providing low-impedance drive to the crystal. Y1 is a fifth-overtone, AT-cut crystal ground for operation in the series-resonant mode with a load capacitance of 30 pF. The feedback path is completed through a resonant circuit consisting of C1, C2 and L1 that selects the desired overtone. R14 loads the drain of Q1 to ensure linear operation. It also sets the loop gain of the oscillator. The dual varactor diode, D1, in series with the crystal, provides for pulling of the crystal frequency by ±500 Hz. L2 cancels out the parallel capacitance of the crystal to enable a wider pulling range.

The circuit composed of D2, R2, R3 and C9 controls the amplitude of the oscillator. The voltage across R3 is about 1.6 V. When the RF voltage on Q1's drain reaches –2 V, D2 conducts, and the signal is limited. This is done without affecting the operating point of Q1, so it remains in a linear, low-noise mode. R2 can be adjusted to change the output level of the oscillator, while making sure that the power

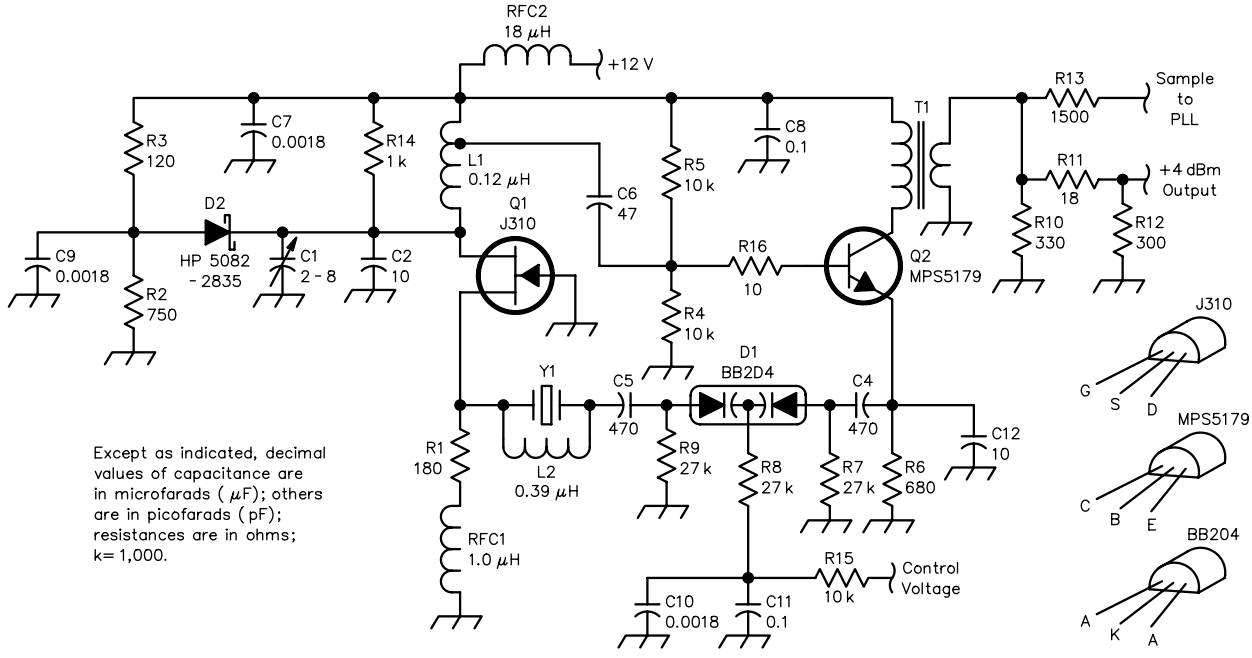

Fig 2—VCXO schematic diagram. Unless otherwise specified, use 1/4 W, 5%-tolerance carbon composition or film resistors.

C1—2-8 pF NP0 ceramic trimmer
C2—10 pF NP0 ceramic disc
L1—0.12 μH, 8 turns #22 AWG enameled wire on T30-12 with a tap 2 turns from cold end
L2—0.39 μH, 15 turns #26 AWG enameled wire on a T37-12 powdered-iron core.
T1—Primary 6 turns #30 AWG enameled wire, secondary 2 turns #28 AWG enameled wire on a BN-61-2402 ferrite core.
Y1—Fifth-overtone crystal, series resonant, 30 pF load capacitance, series resistance less than 60 Ω.

dissipated in Y1 never exceeds 1 mW.

To ensure minimum effect on loop gain by external load variations, the output of the oscillator is taken from the collector of Q2. T1, a 9:1 broadband transformer, provides impedance matching; 6 to 7 dBm is available at its secondary. A 3-dB attenuator provides more isolation and reduces the signal level to prevent overdrive of the next stage in the LO chain. The 1500-Ω resistor is used to couple some of the output to the PLL circuitry.

The PLL Circuit

Fig 3 shows the PLL components required to lock the VCXO frequency to the 10-MHz output of a rubidium frequency standard. A sample of the VCXO output is applied to a dual-modulus prescaler chip, U2. This can be a Motorola MC12019 for division by 20/21, or a Motorola MC12015 for division by 32/33. The prescaler divides the VCXO frequency so that it will not exceed the 20-MHz maximum clock frequency of the PLL chip, U1.

The Motorola MC145158 PLL chip at U1 is the heart of the circuit. It accepts the 10-MHz reference frequency at pin 1 and divides it to a user-settable internal reference frequency using the R-counter. The prescaled VCXO output is applied to pin 8, the input of the A and N counters. The A counter determines when the prescaler will be switched from the N to N+1 mode. The N counter divides the prescaler output before application to the phase detector. The PLL will lock at the frequency determined by all of these counters as shown in Table 1.

The phase-detector output at pin 4 of U1 is filtered by R19 and C13, then amplified by U3. U3 is required to increase the phase detector output, from 5 to 13.5 V. Note that R19 and C13 are *not* the values predicted by the equations Motorola supplies for the PLL. The crystal is a high-Q device and there is a time delay when changing its frequency. The low-pass-filter time constant had to be determined experimentally. The loop has been verified to be adequately damped with three crystals of different manufacture, so the time constant should not need to be changed. To ensure stability, the PLL reference frequency should not be set below 50 kHz. It should also not go above 200 kHz to ensure that the phase-detector output is accurate. This frequency range should be adequate for all amateur microwave and millimeter-wave LO requirements. Choose your division ratios carefully.

The PLL (U1) is configured by data entered serially on the clock, data and enable pins. A PIC16F83 microcon-

Table 1—Frequency vs Divider Values R, A, and N.

MC12019 prescaler: Frequency = (10 MHz / R)×(A + N×20)
MC12015 prescaler: Frequency = (10 MHz / R)×(A + N×32)
Note that *N* cannot be less than the prescaler division ratio.

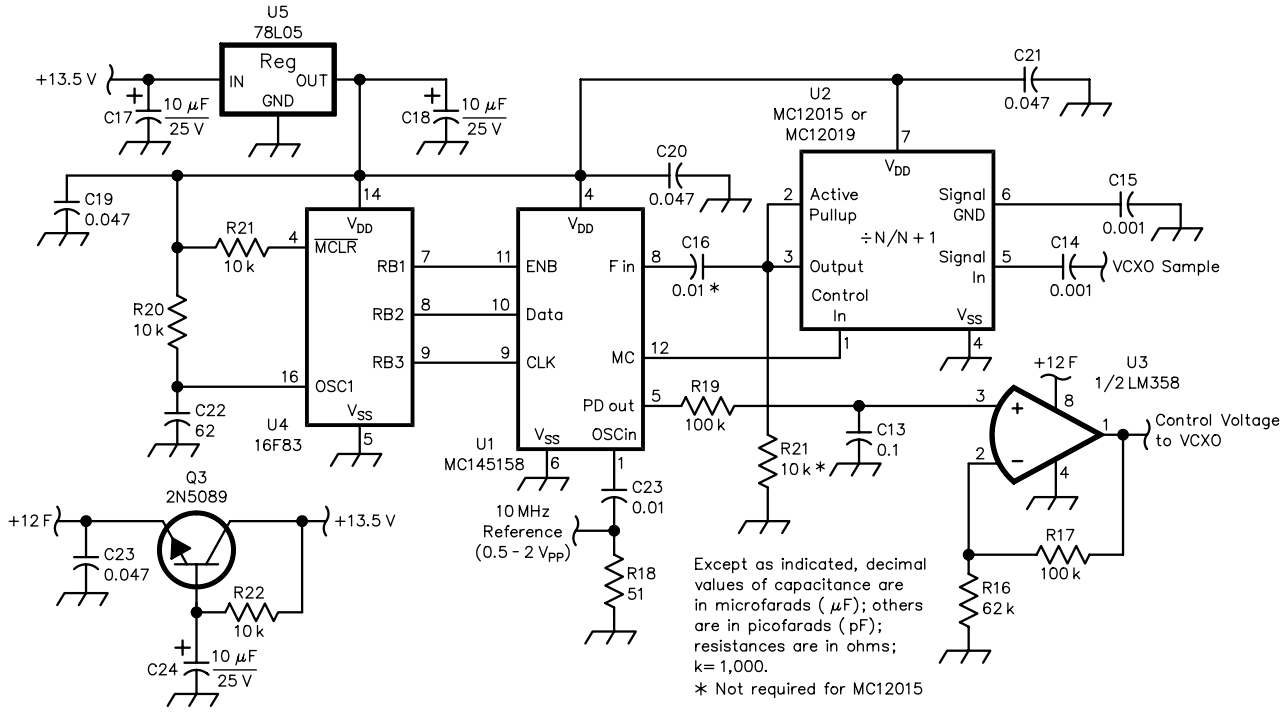

Fig 3—PLL schematic diagram. Unless otherwise specified, use 1/4 W, 5%-tolerance carbon composition or film resistors. C16 and R21 are not required if U2 is a MC12015.

C22—62 pF ceramic, ±10% tolerance
C14-C16, C23—ceramic, ±20% tolerance
C13—Monolithic ceramic, ±20%
C19, C20, C21, C23—Monolithic ceramic, +80%/–20%
C17, C18, C24—Tantalum Electrolytic
U1—MC145158 PLL
U2—MC12019 (∏20/21) or MC12015 (∏32/33) prescaler
U3—LM358
U4—PIC16F83 microcontroller
U5—78L05 5-V regulator

troller unit (U4, MCU) provides these data. Bits 1, 2 and 3 of U4 port B are used to drive these lines. Since the MCU does not require an accurate clock, the RC oscillator configuration is used. The use of an MCU may seem like overkill, but a PIC16F83-04 with 1 KB of program memory and 68 bytes of RAM is only $6.25 in single-unit quantities. The single 18-pin DIP package is also smaller than any other solution.

LO Chain

My 24.192-GHz transverter uses a harmonic mixer with an anti-parallel diode pair that requires injection at half the LO frequency. With a 1296-MHz IF, this works out to 11.448 GHz. Thus, the output of the VCXO at 95.4 MHz needs to be multiplied by 120. I planned to use the same frequency-multiplication chain that N1BWT used in his 10-GHz transverter (see Note 3). This multiplied the crystal frequency by six in the first stage, followed by two stages of multiplication by four and five. Each was a single PC board. However, measurements showed that it degraded the phase noise significantly. The first multiplication in this LO chain reduced the LO signal level below –23 dBm. Coupled with a noise figure of 6 dB, this could not support an LO-to-noise ratio of more than –148 dB—a degradation of 7 dB on the theoretical minimum of –155 dBc.

The LO chain was redesigned to add an additional stage, resulting in successive multiplication by 2, 3, 4 and 5. The KK7B LO board was modified to act as a tripler and a new doubler stage was designed to precede it.

Frequency Doubler

The doubler stage in Fig 4 is essentially a full-wave rectifier. This circuit suppresses the fundamental and odd harmonics,[8] which results in much cleaner output from the following tripler. U1, an MSA-1104, provides the low noise figure and high output level that are critical to maintaining a low noise floor. D1 and D2 are driven with about +16 dBm and produce about +3 dBm of output, which is then filtered by L1 and C2. Minimal filtering is required here, given the six poles of filtering in the tripler that follows.

Frequency Tripler

Modifying a KK7B ×6 multiplier board to perform the tripler function turned out to be fairly easy. Remove U1, Q2 and R7 from the board (see Fig 5) to disable the original crystal oscillator. Connect the doubler output to the free end of C10. Replace U2 with an MSA-0485—less gain is needed, as the input level is larger. It amplifies the +3 dBm from the doubler to +11 dBm, which is enough to drive the following diode tripler. Also, replace L3 with a 0.22 µH RFC.

The original diode sextupler is converted to a tripler by removing L4 and C12 and changing C11 to 8.2 pF. This creates a low-Q series resonant circuit at about 190 MHz to isolate the tripler output from U2. D1 is also removed and replaced with two PIN diodes in anti-parallel. PIN diodes produce about 3 dB more output in this application than Schottky diodes[7]. The anti-parallel circuit also results in 6 dB more output than a single diode and good suppression of even harmonics, resulting in a cleaner LO. I used two ECG-553 diodes because they were easily available, but an HP HSMP-3821 or two 5082-3188s should work just as well. I thought about designing a more complex impedance-matching circuit for the PIN diodes, but tripler output was better than predicted by the HP application note, so I discarded the idea in favor of simplicity.

U3 is replaced with an MSA-0685 to reduce the noise figure. Since the signal levels are much higher, U4 is removed and replaced with a copper strap to the filter. Also remove C15 and R9. Replace C15 with a copper strap and change R10 to a 360-Ω, 1/2-W resistor. U5 can be an MSA-0485 for +12 dBm output or an MSA-1104 for +16 dBm output. The MSA-0485 is adequate to drive the KK7B ×4 multiplier board.

Construction

I built the VCXO and PLL on copper-clad Vectorboard. Make sure to shield the VCXO from the PLL, otherwise leakage from the PLL digital circuitry will show up as spurs at –50 to –60 dBc after multiplication to 11 GHz. One doubler was constructed in a minibox for testing and the other on the KK7B board by chopping up the traces in the old crystal-oscillator area. It could probably be added to the VCXO board.

Circuit construction on copper-clad perfboard was described in amateur literature in the late 70s, but it is less well known today. It requires the use of old-fashioned leaded components, but avoids the need to etch PC boards. I've found that this method can be used up to 150 MHz if care is taken to provide large interconnected areas of copper as a ground plane.

The board I use is made by Vector Electronics.[5] It is an epoxy-glass material with 0.042-inch-diameter holes punched on a 0.1-inch grid and is coated with copper on one side. Components are mounted on the epoxy-glass side and the grounded ends of components are just soldered to the copper. Where ungrounded connections are required, a pad-cutting tool is used to remove the copper around the holes. With good layout, most interconnections in analog circuits can be accommodated by mounting the components in adjacent holes and soldering the leads together on the non-component side of the board. Occasionally, you will need to run a wire between holes to make connections.

MCU Programming

The PIC16F83 MCU must be programmed to load the appropriate values into the MC145158 PLL chip. A listing of the program used may be

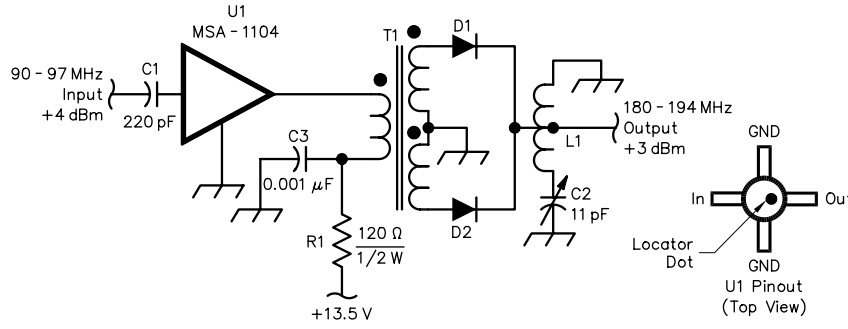

Fig 4—Frequency doubler schematic.

C2—11 pF trimmer
D1, D2—HP5082-2835
L1—6 turns #24 AWG enameled wire 1/4-inch long on a 3/16-inch-diameter form. Tap at 1 1/2 turns from grounded end.
T1—5 trifilar turns #26 AWG enameled wire on a FT37-61 ferrite-toroid core.

downloaded from the ARRL Web page.[10]

The program is very simple. On power up, it initializes the port used to communicate with the PLL, executes a delay routine to ensure that the PLL chip has powered up, programs the PLL registers then shuts off. The PLL counter division values are sent one bit at a time, with the most-significant bit first. In this example, the PLL phase detector runs at 100 kHz, so the R counter is set for division by 100. The N and A counters are set for division by 49 and 15, respectively, to achieve division by 995 when used with a MC12015 prescaler.

The program uses common subroutines to send ones and zeros to the PLL chip and enable latching of the values sent. The program may be easily altered by changing the calls to the subroutines ONE and ZERO to reflect the binary values to be loaded into the counters. For information on programming PIC MCUs, see the October 1998 *QST*.[6]

Adjustment

Adjustment of the LNPLXO is straightforward. Apply power and adjust C1 for maximum output on a power meter. This can be as simple as a 50-Ω resistor, a Schottky diode rectifier and a voltmeter. Then connect the 10-MHz reference oscillator and adjust C1 for approximately 5 V on D2. This detuning pulls the crystal frequency slightly to center it in the PLL lock-in range. Check the power output again to be sure that it has not dropped by more than 0.5 dB. If it has, add a capacitor in series with the crystal to raise the frequency, or an inductor to lower the frequency and repeat the adjustment. Crystals ordered with a 10-ppm tolerance and 30-pF load should not require any circuit modifications. If you have crystals on hand that are calibrated for series resonance without a reactive load (so-called 0-pF load), insert a 100-nH inductor in series with the crystal.

Results

The output at 552 MHz was examined on a spectrum analyzer and all spurious outputs—except the second harmonic—were below –55 dBc, as shown in Table 2.

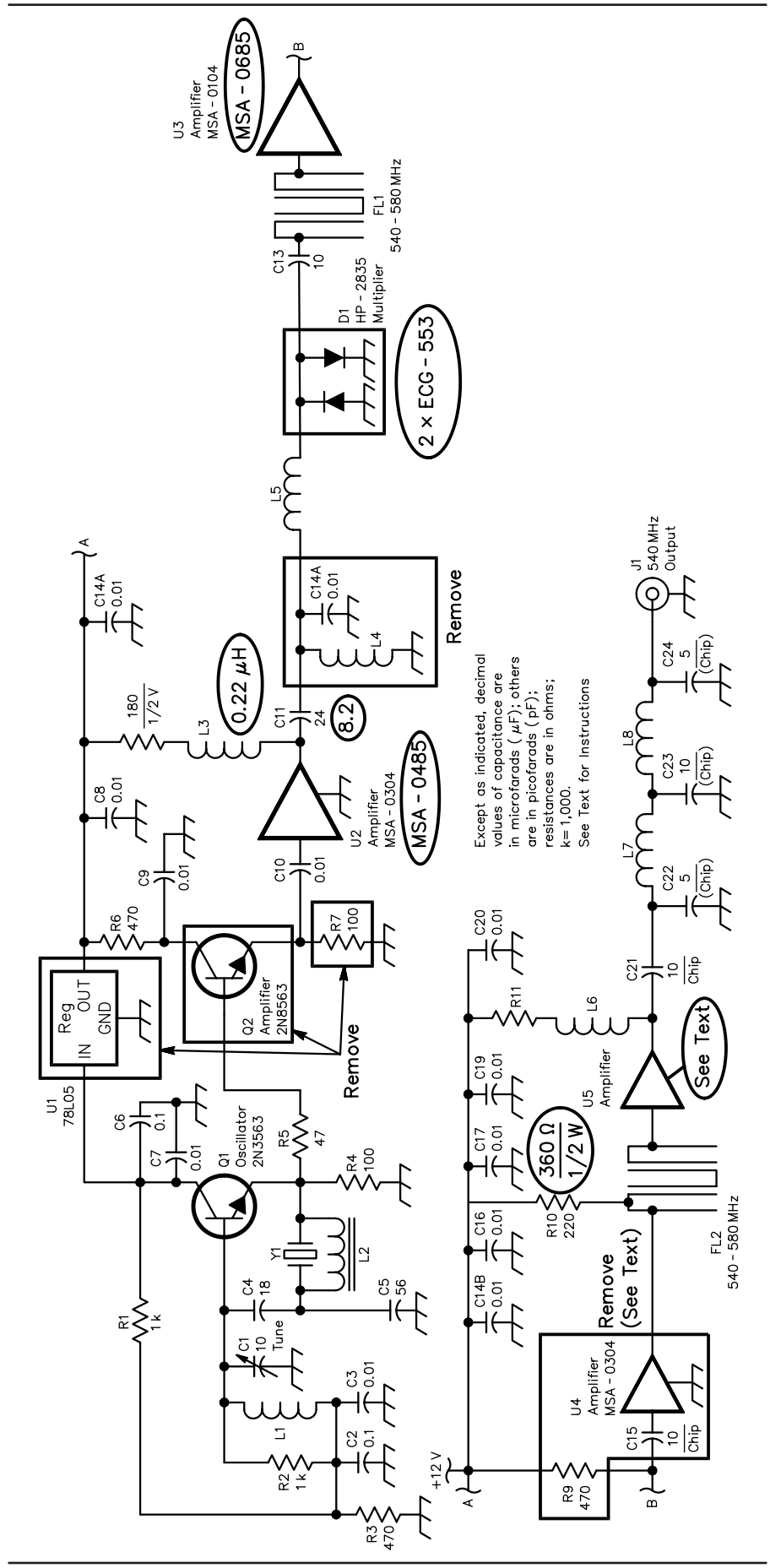

Fig 5—(right) Modifications to convert KK7B's ×6 multiplier into a frequency tripler. Detailed instructions are given in the text.

Table 2—Output Spectrum

Harmonic	*Frequency (MHz)*	*Level (dBc)*
1	92	< –75
2	184	–62
3	276	< –75
4	368	–56
5	460	–70
6	552	0
7	644	< –75
8	736	–67
9	828	< –75
10	920	–72
11	1012	< –75
12	1104	–43

Table 3—SSB Phase Noise at 552 MHz

Offset (kHz)	*Noise (dBc)*
2	–133
5	–143
10	–146
25	–148
50	–150
500	–154

Phase-noise measurement was done by building two identical 92-MHz LNPLXOs and multiplier chains then connecting them to a common 10-MHz crystal oscillator. The outputs (approximately +17 dBm) were then applied to a double balanced mixer (DBM) through 10- and 20-dB attenuators, resulting in a +7 dBm LO and –3 dBm at the RF port. The output of the DBM was ac-coupled to a low-noise amplifier. This arrangement converts the carrier to dc and the phase noise sidebands on each side of the carrier to frequencies between 2 kHz and 500 kHz, where they were measured on a HP 8553 spectrum analyzer. See Note 9 for more information on this technique.

To measure the phase noise in the absence of the multiplier chain, the LNPLXOs were connected to low-noise isolation amplifiers and a level-23 DBM. This DBM did not support an IF below 100 kHz, so measurements were limited to offsets between 100 and 500 kHz.

The noise floor of the basic LNPLXO was measured to be –171 dBc. After multiplication by six to 552 MHz, the noise floor at a 500-kHz offset was measured at –154 dBc. This is very close to the theoretical minimum, considering that my measurements are only accurate within ±2 dB. The phase noise versus frequency for these two cases is shown in Table 3. The SSB phase noise rises slowly from –150 dBc at 50 kHz to –143 dBc at 5 kHz, and then jumps to –133 dBc at 2 kHz. The slow rise is probably caused by flicker noise in the J310 FET and AM-PM conversion in the multipliers. The more rapid rise below 5 kHz occurs within the passband of the crystal itself, and is as expected.

This performance should be adequate for my 24-GHz transverter, which has a noise figure of 1.9 dB and a calculated third-order input intercept of –28 dBm. This would result in a two-tone dynamic range of 76 dB with a perfect local oscillator. I estimate that the LO phase-noise floor will degrade by 34 dB (32 dB for multiplication by 40, plus an extra 2 dB for circuit losses) to –120 dBc after multiplication to 22.896 GHz. This would limit dynamic range to 78 dB in a 16-kHz bandwidth, so LO noise is not the limiting factor for NBFM, SSB and CW operation on the 12-mm band.

Low LO phase noise will be even more important for the 6-mm band, where LO phase noise will degrade by 7 dB, reducing the dynamic range to 71 dB. This results in a dynamic range at 47 GHz that is similar to that of 10-GHz transverters using the traditional Butler oscillator circuit. In addition, the frequency will stay within 50 Hz—even if it is 115° in the shade.

Notes

[1]H. Neidel, DL1IN, "First QSO on 411 GHz," *DUBUS*, 2/98, p 44.

[2]R. Campbell, KK7B, "A Clean, Low-Cost Microwave Local Oscillator," *QST*, July 1989, pp 15-21.

[3]P. Wade, N1BWT, "Building Blocks for a 10-GHz Transverter," *ARRL UHF/Microwave Projects Manual*, Vol 2, pp 3-33 to 3-40.

[4]I use a surplus Efratom FRK-L rubidium oscillator obtained from Lehman Scientific, 85 Surrey Dr, Wrightsville, PA 17368. They will also perform calibration of oscillators, traceable to NIST. Don't try to calibrate these using WWV or WWVH. Received WWV and WWVH signals are only accurate to 0.1 ppm because of propagation variations caused by short-term instability of the ionosphere. These used oscillators sell for about $500.

[5]Vector Electronics products are available from most distributors and some local electronic parts stores in the US. Vector part number 169P84WEC1 is a 17× 8.5-inch board. Vector part number P138 is a pad-cutting tool.

[6]J. Hansen, W2FS, "Using PIC Microcontrollers in Amateur Radio Projects," *QST*, Oct 1998, pp 34-40.

[7]*Low Cost Frequency Multipliers Using Surface Mount PIN Diodes*, Application Note 1054, Hewlett Packard. (A PDF file of this note is available at **http://ftp.hp.com/pub/accesshp/HP-COMP/rf/4_downld/lit/diodelit/an1054.pdf**.—*Ed.*)

[8]W. Hayward, W7ZOI and D. DeMaw, W1FB, *Solid-State Design for the Radio Amateur*, p 42.

[9]V. Manassewitsch, *Frequency Synthesizers—Theory and Design* (New York: John Wiley and Sons, 1987).

10. You can download this package from the ARRL Web **http://www.arrl.org/files/*qex*/**. Look for STEP1199.ZIP.

John Stephensen, KD6OZH, has been interested in radio communications since building a crystal radio kit at age 11. He went on to study Electronic Engineering at the University of California and has worked in the computer industry for 26 years. He was a cofounder of Polymorphic Systems, a PC manufacturer, in 1975 and a cofounder of Retix, a communication software and hardware manufacturer, in 1986. Most recently, he was Vice President of Technology at ISOCOR, which develops messaging and directory software for commercial users and ISPs.

John received his Amateur Radio license in 1993. He is active on amateur bands from 28 MHz through 24 GHz. His interests include designing and building Amateur Radio gear, operation through digital and analog amateur satellites, VHF and microwave contesting and 10-meter DX. His home station is almost entirely homebrew and supports operation on SSB, PSK31, RTTY and analog and digital satellites in the 28, 50, 144, 420, 1240, 2300, 5650 and 10,000 MHz bands from grid square DM04 in Los Angeles. The mobile station includes 10-meter SSB, 144/440 MHz FM and 24 GHz SSB.